

Electronic, Chemical and Structural Properties of Metamorphic III-V Compound Heterojunctions & Devices: DMR-0313468

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•The objective of this FRG program is to explore the properties of lattice-engineered, multi-layered compound semiconductor structures so that a new class of “metamorphic” semiconductor materials can be developed, for which unprecedented electronic and optical properties are accessible without structural constraints imposed by common substrates. The relations between nano-scale chemical, structural, growth and electronic properties are explored by an interdisciplinary team, and devices are fabricated to exploit new properties and to provide feedback for materials growth.

•The figures show a progression from demonstrating super-low defect content mismatched InGaAs (fig. 1) and ideal lattice relaxation of the InGaAs layer (fig. 2), to demonstrating device-quality material with extremely long carrier lifetimes that demonstrate true device viability for these defect-engineered heterostructures (fig. 3) and to our first fabricated ultra-high speed transistor (fig.4) using these novel materials.

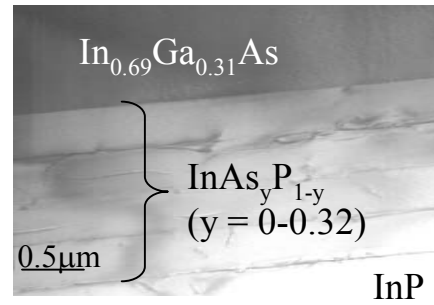


Fig. 1. Cross-sectional transmission electron micrograph of low defect density, lattice-mismatched (metamorphic) InGaAs on graded InAsP/InP.

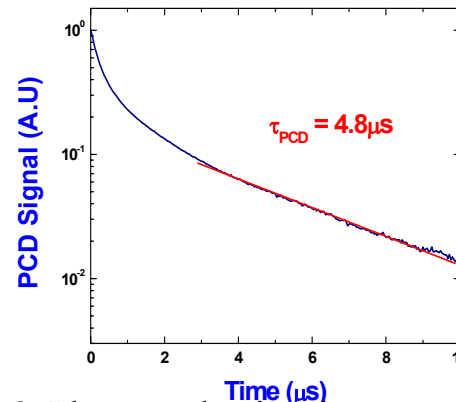


Fig. 3. Photoconductive decay response of lattice-mismatched InGaAs @ $E_g = 0.6$ eV with recombination lifetime of ~ 5 usec, very close to the theoretical maximum of 7 usec for the case of no defects.

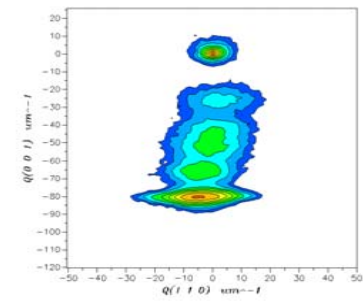


Fig. 2. Reciprocal space x-ray diffraction map indicating near ideal lattice relaxation of high-mismatched InAsP-InGaAs.

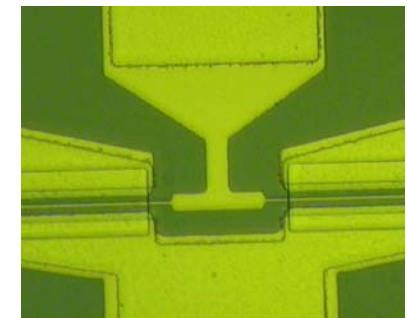


Fig. 4. Topview of a fully fabricated InGaAs/InAsP composite channel high electron mobility transistor (CH-HEMT) using metamorphic InAsP buffers.

Figure 1. Cross sectional TEM image of an MBE-grown step graded InAsP buffer on InP, capped with an InGaAs layer whose lattice constant is designed to match that of the last InAsP layer. The goal here is to exploit the use of anion based lattice grading by slowly increasing the As content as opposed to the P content, thereby increasing the overall layer lattice constant via compressive strain relaxation. The reason for using the anion lattice is to decouple the strain introduction rate (via compositional change) and the growth rate (via In flux) since growth rate will affect the efficiency of strain relaxation otherwise. We have shown in a past NSF program that using the cation for such lattice grading introduces substantially higher defect (dislocation) concentrations than shown in figure 1, for which no dislocations are evident at the TEM scale in the relaxed InGaAs overlayer (other methods reveal the dislocation density to be $\sim 2\text{-}3 \times 10^6 \text{ cm}^{-2}$, which is very low). The perfection of the InGaAs/InAsP interface from a structural perspective is evident, and this is backed up by nanoscale cathodoluminescence measurements (not shown) of this interface which measured the change in band offsets. This work is the subject of 3 APL papers and two conference papers.

Figure 2 is a reciprocal space map obtained using triple axis XRD, from which analysis indicates that the strain relaxation of each layer shown in figure 1 is nearly fully relaxed ($>90\%$) with no lattice tilt and very sharp diffraction peaks for each layer that are clearly distinct in the figure. We have performed extensive modeling and analysis of the strain relaxation modes in this system and we have demonstrated from this data that these layers which are grown on offcut (001) InP substrates, relax symmetrically in 2 dimensions due to the differences in glide velocity of orthogonal misfit dislocations which offset the impact of substrate miscut. With such an understanding and measurement, we are expanding knowledge of the InAsP anion grading for the purpose of achieving an engineered substrate with arbitrary lattice constant between InP and InAs. This work is the subject of 1 APL paper, 1 JAP paper and one conference paper.

Figure 3 shows the PCD response of an InAsP/InGaP/InAsP double heterostructure that is grown to be lattice matched to the top InAsP layer of figure 1. The purpose is to see whether the level of structural perfection achieved in figures 1 and 2 translates into high electronic quality material, since point defects generated by such lattice relaxation is not understood in this system. From the data, extremely long recombination lifetimes are achieved, that are near the theoretical maximum for this material. This demonstrates that point defects are well absorbed into the growing lattice and the material at this composition, which is approximately 1.15% mismatched with respect to InP, is ready for device use. Not shown is a complete study of carrier mobility in these mismatched materials. These works are the subject of a submitted APL, a submitted JAP and 2 conference papers.

Figure 4 shows a top view picture of a very recently fabricated HEMT that incorporates a graded InAsP buffer for the first time, so that a novel composite heterostructure channel device can be fabricated. To date, this structure was only a theoretical construct and we are in the process of analyzing the device performance for future development and feedback into our growth process for continued optimization and ejection of device technology from this materials research program.

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Education:

Five graduate students (Yong Lin, Shawn Bradley, Dongmin Liu, Mykola Bataiev and Phil Smith) and 5 undergraduate students (Andrew Carlin, Drew Malonis, Steve Barr, Kaden Hazzard and Joe Gorse), some with REU support, are contributing to this FRG program. Barr, Hazzard and Carlin are moving on to graduate school (Carlin is staying at OSU in a combined BS/MS fast-track program), while Malonis and Barr are continuing their undergraduate studies. Our MBE engineer, Mark Brenner, is performing his MS on this project while working full time in the lab.

Outreach:

- This FRG combines extremely diverse student researchers, including undergraduate physics students working on theoretical models (they have published six (!) papers, including a Phys. Rev. Lett.), graduate and undergraduate students in EE and Physics working together on nano-scale interface studies, device modeling/design/fabrication, materials growth and characterization. Multiple joint papers and conference talks have already been published and several more have been submitted for review.

- Our MBE engineer on this project, Mark Brenner, and Ringel have given 6 tours (20 students each) of FRG lab facilities and demonstrations to the 2003 Freshman Introduction to Engineering Class as part of a program to achieve freshman immersion into nanotechnology for ALL areas of engineering.